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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte PAUL SILVESTRI and JONATHON G. GREENWOOD

Appeal 2016-000123
Application 12/400,632[1]
Technology Center 2800

Before ADRIENE LEPIANE HANLON, CATHERINE Q. TIMM, and JAMES C. HOUSEL, *Administrative Patent Judges*.

PER CURIAM.

DECISION ON APPEAL

A. STATEMENT OF THE CASE

Appellants filed an appeal under 35 U.S.C. § 134(a) from the Examiner's decision finally rejecting claims 1, 3, 5, 6, 8, 10, 11, 17, and 19–29.[2] We have jurisdiction under 35 U.S.C. § 6(b).[3]

We REVERSE.

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[1] According to Appellants, the real party in interest is Micron Technology, Inc. Br. 1.

[2] Claims 7 and 18 have been withdrawn from consideration and are not before us on appeal.

[3] Our decision refers to the Appellants' Specification filed Mar. 9, 2009 (Spec.), the Final Office Action mailed Aug. 11, 2014 (Final Act.), the Appeal Brief filed Feb. 11, 2015 (Br.), and the Examiner's Answer mailed July 10, 2015 (Ans.).

The subject matter on appeal relates to microelectronic devices (*see, e.g.*, claims 1, 17, 26). Microelectronic devices are required to have ever higher performance and smaller packaging. Spec. ¶ 2. One way to address this demand is to stack microelectronic dies so more computing power or memory is provided within the same unit of space or footprint. *Id.* Although this technique reduces the amount of space used by larger devices, the effectiveness of the technique is limited to a certain height, depending upon the device and its use. *Id.* For instance, longer wirebonds between the upper die(s) and a lead frame or interposer substrate lead to increased latency. *Id.* ¶¶ 2, 3. Further, using a logic component in a device adds functionality but also adds another die that increases the height of the die stack. *Id.* ¶ 3. Vias may be used to interconnect dies to one another and a substrate, as well as to connect a logic component when one is present. *Id.* ¶ 4. However, although vias mitigate latency problems, they are more expensive than wirebonds. *Id.*

In view of the above, Appellants disclose there is a need for cost-effective structural arrangements that can reduce latency and the overall size of microelectronic devices. *Id.* Figure 5 of Appellants' disclosure is reproduced below.

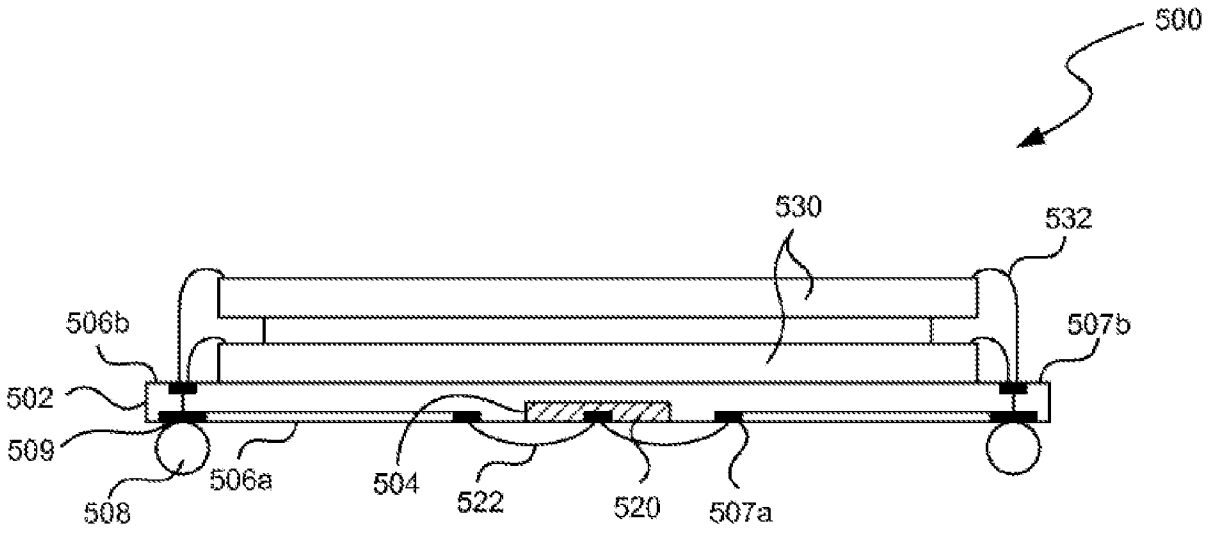

FIG. 5

Figure 5 is a cross-sectional view of a microelectronic device.

Figure 5 depicts a microelectronic device 500 including an interposer substrate 502 and a recess defined by a blind hole 504 extending from a first side 506a of the interposer substrate 502 to an intermediate depth within the interposer substrate 502 but not completely through the substrate 502. *Id.* ¶ 20. A logic component 520 is positioned in the blind hole 504, which can vary in depth and width to accommodate logic components of different sizes so the logic component 520 is substantially flush with the first side 506a of the substrate 502. *Id.* ¶ 21. The logic component 520 is connected to bond pads 507a by wirebonds 522 and the device 500 further includes one or more dies 530 connected to bond pads 507b by wire bonds 532. *Id.* ¶¶ 21, 22.

Independent claim 1 is illustrative and is reproduced below from the Claims

Appendix of the Appeal Brief.[4] The limitations at issue are italicized.

1. A microelectronic device, comprising:

an interposer substrate having a first side and a second side, *a recess open at the first side and extending partially, but not completely, through the interposer substrate, the recess having a base* and recess sidewalls at least generally transverse to the first side, the interposer substrate further having a plurality of first terminals at the first side, and a plurality of second terminals at the second side;

one or more individual dies attached to the second side of the interposer substrate, the one or more individual dies having integrated circuitry and bond sites electrically connected to the second terminals of the interposer substrate; and

a logic component having a major surface and logic component sidewalls at least generally transverse to the major surface, *the logic component being in the recess* at the first side of the interposer substrate and attached to the base of the recess of the interposer substrate, the logic component is electrically connected to the second terminals at the second side,

wherein—

the base has a first width between the recess sidewalls,

the major surface has a second width between the logic component sidewalls, and

the first width is generally the same as the second width.

The claims on appeal stand rejected as follows:

(1) claims 1, 5, 6, 11, and 26 under 35 U.S.C. § 103(a) as unpatentable over Wallace[5] in view of Suh;[6]

(2) claims 3 and 10 under 35 U.S.C. § 103(a) as unpatentable over Wallace in view of Suh and further in view of Mehta;[7]

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[4] Br. Claims Appendix 20.
[5] Wallace, US 6,639,309 B2, issued Oct. 28, 2003 ("Wallace").
[6] Suh, US 7,911,065 B2, issued Mar. 22, 2011 ("Suh").
[7] Mehta et al., US 2008/0054435 A1, published Mar. 6, 2008 ("Mehta").

(3) claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Wallace in view of Suh and further in view of Kim;[8]

(4) claims 22 and 23 under 35 U.S.C. § 103(a) as being unpatentable over Wallace in view of Suh and further in view of Jang;[9]

(5) claims 27–29 under 35 U.S.C. § 103(a) as being unpatentable over Wallace in view of Suh and further in view of Wehrly;[10]

(6) claims 17 and 19–21 under 35 U.S.C. § 103(a) as being unpatentable over Wallace in view of Mehta and Suh; and

(7) claims 24 and 25 under 35 U.S.C. § 103(a) as being unpatentable over Wallace in view of Mehta and Suh and further in view of Jang.

B. DISCUSSION

Rejection over Wallace and Suh

Claims 1, 5, 6, 11, and 26 are rejected under 35 U.S.C. § 103(a) as unpatentable over Wallace in view of Suh. We select claim 1 as representative for discussing the issues on appeal.

The dispositive issue on appeal is whether the combination of Wallace and Suh discloses or suggests a microelectronic device comprising an interposer substrate recess and a logic component, wherein the width of the base of the recess between its sidewalls is "generally the same" as the width of a major surface of the logic component between its sidewalls, as recited in claim 1.

The Examiner finds Wallace discloses a microelectronic device. Final Act. 5. Specifically, the Examiner cites Figures 3 and 4 of Wallace. *Id.* Figure 3 of Wallace is reproduced below.

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[8] Kim, US 7,446,420 B1, issued Nov. 4, 2008 ("Kim").
[9] Jang et al., US 6,833,619 B1, issued Dec. 21, 2004 ("Jang").
[10] Wehrly et al., US 2007/0158811 A1, published July 12, 2007 ("Wehrly").

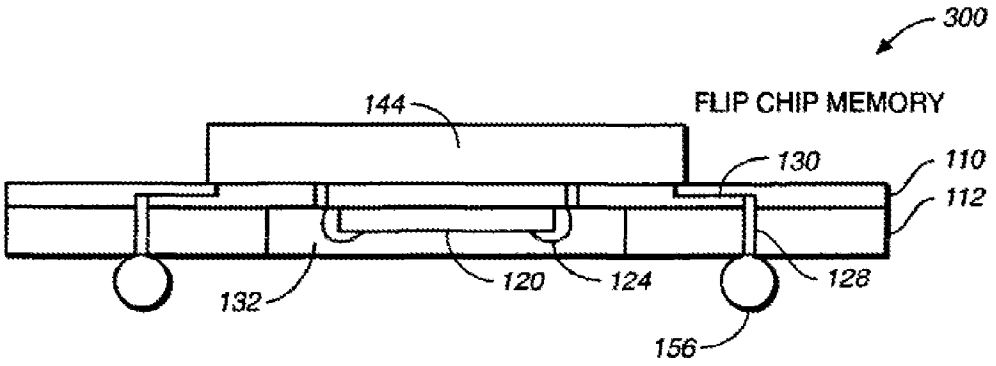

FIG._3

Figure 3 is a cross-sectional view of a chip package.

Figure 3 depicts a memory package 300 including a memory die 144 flip chip bonded to a printed circuit board (PCB) 110. Wallace col. 3, ll. 26–33. The memory die 144 is further connected to a controller die 120 by vias and conductive layers of PCBs 110, 112. *Id.* at col. 3, ll. 33–35. As in previous embodiments of Wallace, the controller die 120 is located within a rectangular hole or central recess of PCB 112, which may be filled with encapsulant 132. *Id.* at col. 2, l. 42 to col. 3, l. 2 and col. 3, ll. 28–38. Figure 4 of Wallace is reproduced below.

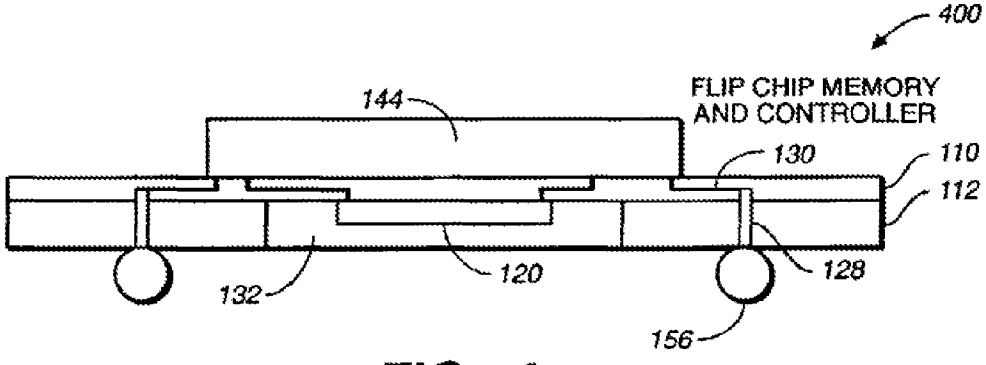

FIG._4

Figure 4 is a cross-sectional view of a chip package.

Wallace discloses that the memory package 400 of Figure 4 is similar to the memory package 300 of Figure 3 except both the memory die 144 and the controller die 120 are flip chip bonded to PCB 110. *Id.* at col. 3, ll. 38–42.

The Examiner finds the devices shown in Figures 3 and 4 of Wallace each include an interposer substrate (i.e., PCBs 110, 112) having a recess (i.e., the rectangular hole or central recess of a PCB in which the controller die 120 is located) open at a first side and extending partially, but not completely, through the interposer substrate and a logic component (i.e., the controller die 120). Final Act. 5.

The Examiner finds Wallace does not explicitly disclose that the width of a base of the recess is "generally the same" as the width of a major surface of the logic component. *Id.* at 6. The Examiner finds Suh discloses that a width of a chip is generally the same as the width of a cavity in which the chip is located. *Id.* The Examiner concludes it would have been obvious to modify the device of Wallace to use the width relationship disclosed by Suh because it would require less encapsulation and reduce manufacturing costs. *Id.*

Appellants contend Wallace does not disclose the width relationship between the width of the recess and the width of the logic component recited in claim 1 because the recess shown in the drawings of Wallace is substantially larger than Wallace's controller die. Br. 8–9. Furthermore, Appellants argue one of ordinary skill in the art would have understood the meaning of the language "generally the same" as "similar to the expression 'equal to,' but without being limited to the very strict definition of 'exactly equal to.'" *Id.* at 9. In particular, Appellants argue:

> [O]ne of ordinary skill in the art of microelectronic device fabrication would understand the meaning of "generally the same" in the context of claim 1 would include small and expected variations in dimensions

> due to, e.g., manufacturing limitations, such as limitations in tolerances associated with etching and/or photolithography, used to form the recess and/or logic component of claim 1.

Id. at 10. To support this argument, Appellants cite Figure 5 and paragraph 21 of Appellants' Specification. *Id.*

The Examiner finds the devices depicted in Figures 3 and 4 of Wallace each include a recess having a width that is "generally the same" as the width of the controller die 120 because Appellants' Specification does not define "generally the same as" as meaning "equal to." Ans. 2. We do not agree with the Examiner because this interpretation essentially renders the language "generally the same" meaningless and removes it from claim 1. Moreover, Figure 5 of Appellants' disclosure depicts a logic component 520 that has a width essentially equal to the width of the blind hole 504 the logic component 520 is located within.[11] Therefore, Figure 5 supports Appellants' definition of "generally the same" as meaning "equal to" but with some small and expected variations in dimensions, such as those created by the manufacturing processes for the logic component and/or recess.

Further, the Examiner reversibly erred by finding the recesses of the devices depicted in Figures 3 and 4 of Wallace have a width that is "generally the same" as the width of the controller die 120. As shown in Figures 3 and 4 above, the width of the recess (which is filled with encapsulant 132) that the controller die 120 is located within is significantly different from the width of the controller die 120. Thus, the width of the controller die 120 is not "generally the same," as that phrase

[11] Paragraph 21 of the Specification discloses the logic component 520 can be "flush" with a side of the substrate 502, but it is first side 506a, or bottom side, of the substrate 502 that the logic component 520 is flush with. In other words, this regards a different dimension of the logic component 520 than the width of the logic component 520 and its relationship to the width of the blind hole 504.

is defined in the previous paragraph, as the width of the recess, when considering the amount of small and expected variations in dimensions one would expect from the manufacturing processes to make the controller die 120 and/or the recess.

The Examiner further relies on Suh, finding Suh discloses a recess within the surface of layer 130 that has the same width as the die 120 located within the recess. Ans. 3. Appellants assert Suh does not disclose a recess within an interposer substrate, as recited in claim 1, because the substrate 110 of Suh lacks any recess. Br. 11. Instead, the semiconductor die 120 is located on top of a base substrate 110 and an insulating pattern 130 is formed over the die 120. *Id.* at 10.[12] Thus, Suh does not disclose a relationship between a width of the chip 120 and the width of a recess in a substrate (i.e., base substrate 110) that the chip is located within, as recited in claim 1. As discussed above, Wallace also does not disclose or suggest this relationship. As a result, modifying Wallace in view of Suh would not result in a recess having a base with a width that is "generally the same" as the width of a major surface of a logic component, as recited in claim 1. For these reasons, we do not sustain the § 103 rejection of claim 1 over Wallace in view of Suh.

Claims 5, 6, and 11 depend from claim 1. Independent claim 26 recites that a major surface of a logic component and a base of a recess in an interposer substrate "have generally similar dimensions." Appellants do not argue claim 26

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[12] Appellants refer to Figure 10 of Suh at pages 10–11 of the Appeal Brief. The Examiner notes at page 3 of the Examiner's Answer that the Examiner cited Figure 7 in the rejection, not Figure 10. However, Figures 8–16 of Suh depict steps in a method to fabricate the semiconductor package disclosed by Suh. Suh col. 10, ll. 23–26. It appears Appellants selected Figure 10 for ease of viewing because it depicts the semiconductor chip 120 after it has been placed on the base substrate 110 and the insulation layer 130 has been formed over the base substrate 110 but before the additional structures depicted in Figures 7 and 16 have been made.

separately from claim 1. Br. 14. Therefore, we construe the language "generally similar dimensions" in claim 26 the same as the language "generally the same" in claim 1 and do not sustain the § 103 rejection of claim 26 over Wallace in view of Suh for the reasons discussed above.

In view of the above, the § 103(a) rejection of claims 1, 5, 6, 11, and 26 under 35 U.S.C. § 103(a) as unpatentable over Wallace in view of Suh is not sustained.

Rejections of Claims 3, 8, 10, 17, 19–25, and 27–29

The rejections of claims 3, 8, 10, 17, 19–25, and 27–29 include Wallace and Suh as references as well as Mehta, Kim, Jang, and Wehrly as additional references. However, the Examiner does not rely upon Mehta, Kim, Jang, or Wehrly to cure the deficiencies of Wallace and Suh. For example, in the rejection of independent claim 17, the Examiner finds Wallace is silent with regard to a plurality of dies in a stack and a planform area of a logic component being generally the same as the planform area of a recess of an interposer substrate. Final Act. 11. For the reasons discussed above with regard to claim 1, Wallace does not disclose or suggest a logic component having a planform area that is "generally the same" as a planform area of a recess, as recited in claim 17. The Examiner relies upon Mehta as disclosing a plurality of dies in a stack and therefore does not rely upon Mehta to cure the deficiencies of Wallace and Suh. In fact, similar to the rejection of claim 1 discussed above, the Examiner finds Suh discloses a chip having a planform area generally the same as the planform area of a recess. *Id.* at 11–12. However, for the same reasons discussed above with regard to claim 1, Suh does not disclose a relationship between a planform area of a logic component and the planform area of a recess of an interposer substrate.

Therefore, although the remaining § 103 rejections rely on additional prior art references, the Examiner does not rely on these additional references to remedy the deficiencies in the combination of Wallace and Suh. As a result, the § 103(a) rejections of claims 3, 8, 10, 17, 19–25, and 27–29 are also not sustained.

C. DECISION

The decision of the Examiner is reversed.

REVERSED